

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,845,458 B2  
APPLICATION NO. : 10/731679  
DATED : January 18, 2005  
INVENTOR(S) : Feng Lin

Page 1 of 8

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the TITLE page, Item (54) please change the title from "SYSTEM AND METHOD OF OPERATION OF DLL AND PLL TO PROVIDE TIGHT LOCKING WITH LARGE RANGE, AND DYNAMIC TRACKING OF PVT VARIATIONS USING INTERLEAVED DELAY LINES"

and insert therefore -- SYSTEM AND METHOD OF OPERATION OF DLL (DUAL LOCKED LOOP) AND PLL (PHASE LOCKED LOOP) TO PROVIDE TIGHT LOCKING WITH LARGE RANGE, AND DYNAMIC TRACKING OF PVT VARIATIONS USING INTERLEAVED DELAY LINES --.

The title page, showing the illustrative figure, should be deleted and substitute therefore the attached title page.

The drawing sheets, consisting of Figs 1-10, should be deleted to be replaced with drawing sheets consisting Figs. 1-10, as shown on the attached pages.

In the text, correct the following:

Column 1:

lines 1-5, delete "SYSTEM AND METHOD OF OPERATION OF DLL AND PLL TO PROVIDE TIGHT LOCKING WITH LARGE RANGE, AND DYNAMIC TRACKING OF PVT VARIATIONS USING INTERLEAVED DELAY LINES" and insert -- SYSTEM AND METHOD OF OPERATION OF DLL (DUAL LOCKED LOOP) AND PLL (PHASE LOCKED LOOP) TO PROVIDE TIGHT LOCKING WITH LARGE RANGE, AND DYNAMIC TRACKING OF PVT VARIATIONS USING INTERLEAVED DELAY LINES --.

line 66, before "phase" insert -- or --.

Column 2:

line 2, delete "rang" and insert therefore -- range --.

line 47, after "device" insert -- ; --.

Column 3, line 5, delete "if" and insert therefore -- in --.

Column 4, line 17, delete "is".

In the claims, correct the following:

Column 7:

claim 1, line 14, delete "o" and insert therefore -- of --.

claim 2, line 3, delete "intrinic" and insert therefore -- intrinsic --.

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 8:

claim 17, line 2, delete "as" and insert therefore -- has --.  
claim 19, line 8, after "circuit" insert -- path --.  
claim 19, line 8, delete "the" first occurrence.  
claim 19, line 13, delete "in".  
claim 21, line 10, delete "track" and insert -- tracks --.  
claim 21, line 18, delete "o" and insert -- of --.

Column 9, claim 28, line 3, delete "de ay" and insert therefore -- delay --.

Column 10, claim 39, line 12, after "circuit" insert -- path --.

Column 11:

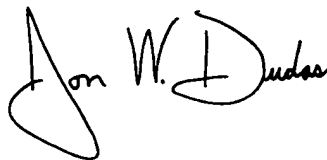
claim 42, line 5, delete "trinsic" and insert therefore -- intrinsic --.  
claim 43, line 8, delete "an" and insert therefore -- and --.  
claim 44, line 7, delete "associate" and insert therefore -- associated --.  
claim 46, line 11, delete "an" and insert therefore -- and --.

Column 12:

claim 47, line 9, delete "an" and insert therefore -- and --.  
claim 49, line 12, delete "an" and insert therefore -- and --.

Signed and Sealed this

First Day of July, 2008



JON W. DUDAS  
*Director of the United States Patent and Trademark Office*

(12) **United States Patent**  
Lin

(10) Patent No.: **US 6,845,458 B2**  
(45) Date of Patent: **Jan. 18, 2005**

(54) **SYSTEM AND METHOD OF OPERATION OF DLL AND PLL TO PROVIDE TIGHT LOCKING WITH LARGE RANGE, AND DYNAMIC TRACKING OF PVT VARIATIONS USING INTERLEAVED DELAY LINES**

(75) Inventor: **Feng Lin, Boise, ID (US)**

(73) Assignee: **Micron Technology, Inc., Boise, ID (US)**

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/731,679**

(22) Filed: **Dec. 9, 2003**

(65) **Prior Publication Data**

US 2004/0119512 A1 Jun. 24, 2004

**Related U.S. Application Data**

(62) Division of application No. 09/652,632, filed on Aug. 31, 2000.

(51) Int. Cl.<sup>7</sup> ..... **G06F 1/12**

(52) U.S. Cl. .... **713/401; 713/400; 713/401; 713/500; 713/503; 327/147; 327/149; 327/157; 327/158; 327/161**

(58) Field of Search ..... **713/400, 401, 713/500, 503; 327/147, 149-163; 716/6; 375/375-376**

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*Primary Examiner*—Lynne H. Browne

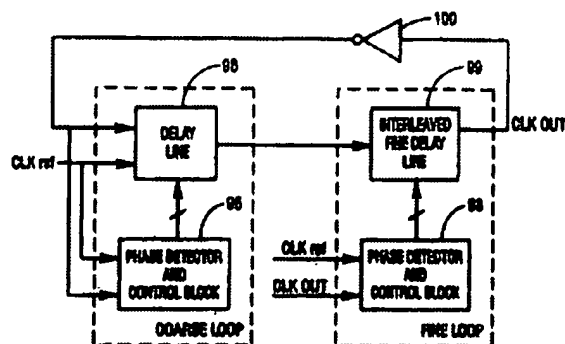
*Assistant Examiner*—Nitin C. Patel

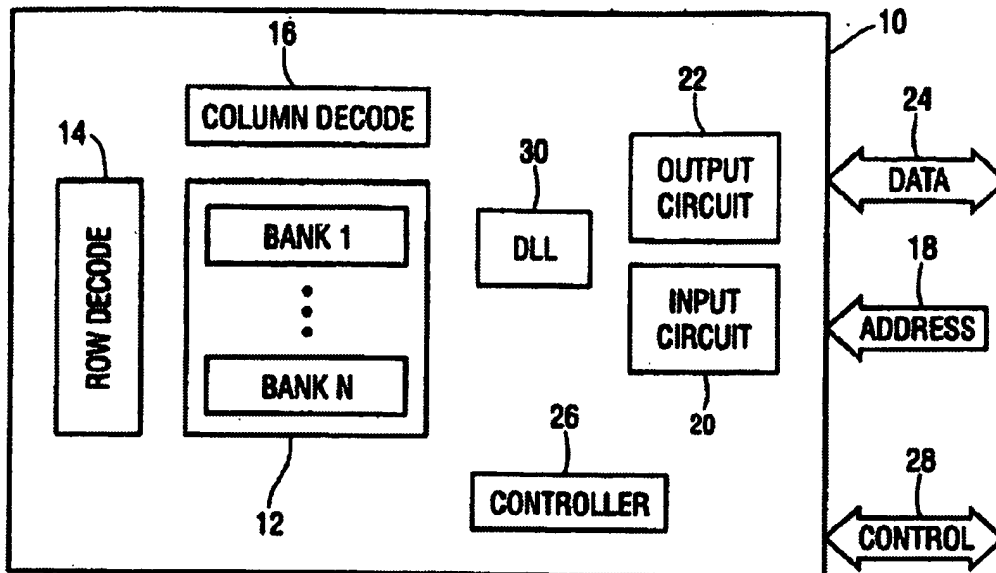
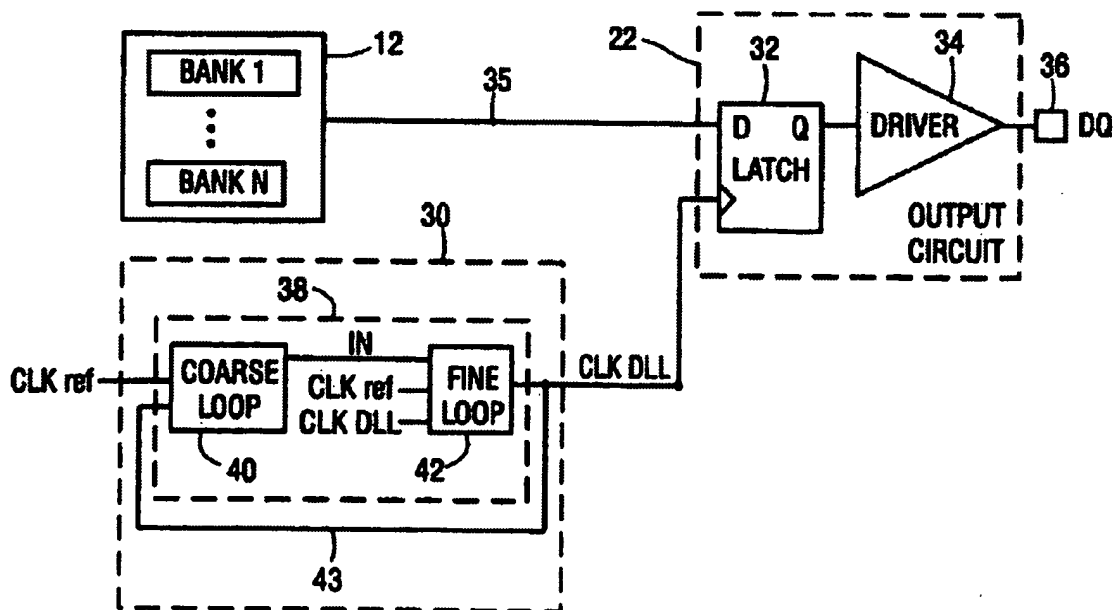
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(57) **ABSTRACT**

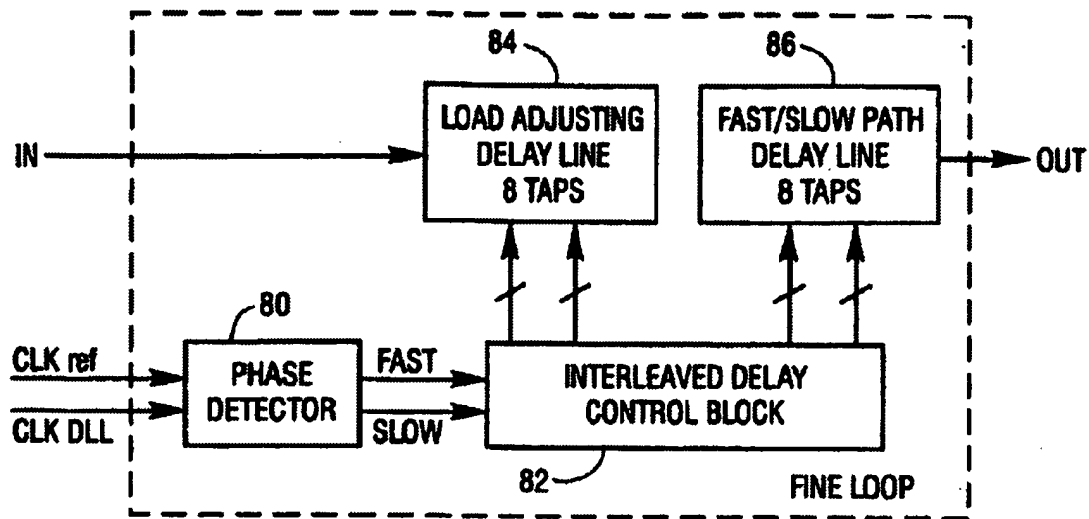
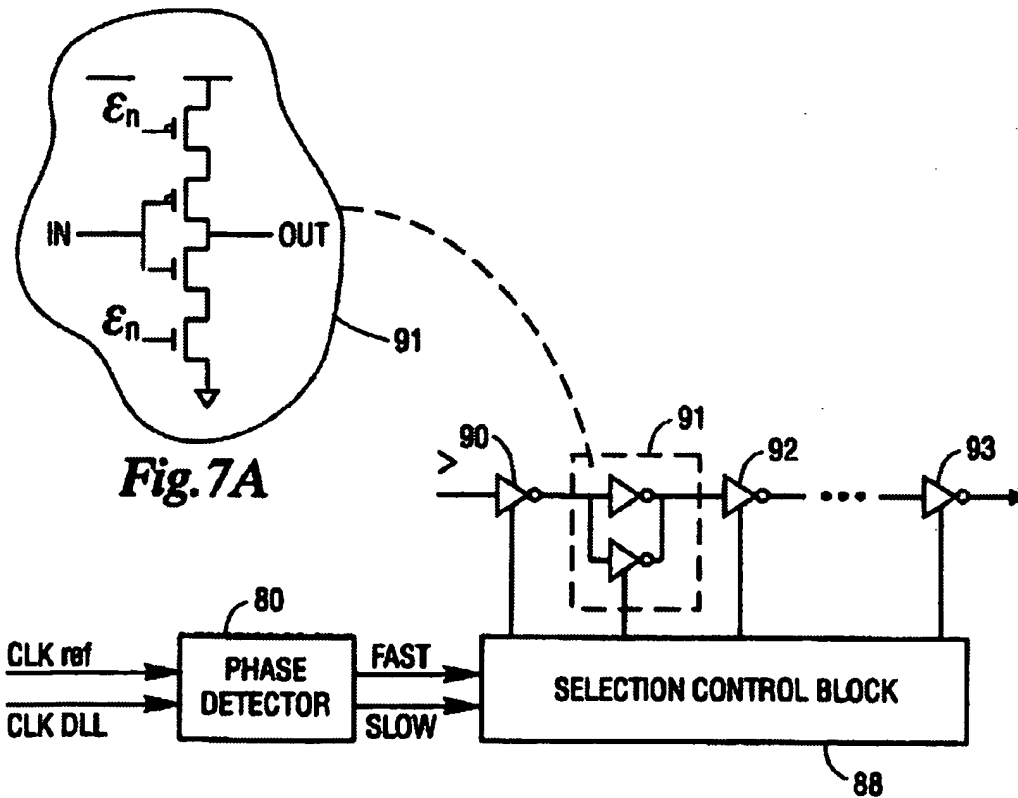
An interleaved delay line for use in phase locked and delay locked loops is comprised of a first portion providing a variable amount of delay substantially independently of process, temperature and voltage (PVT) variations while a second portion, in series with the first portion, provides a variable amount of delay that substantially tracks changes in process, temperature, and voltage variations. By combining, or interleaving, the two types of delay, single and dual locked loops constructed using the present invention achieve a desired jitter performance under PVT variations, dynamically track the delay variations of one coarse tap without a large number of delay taps, and provide for quick and tight locking. Methods of operating delay lines and locked loops are also disclosed.

**50 Claims, 5 Drawing Sheets**



*Fig. 1**Fig. 2*



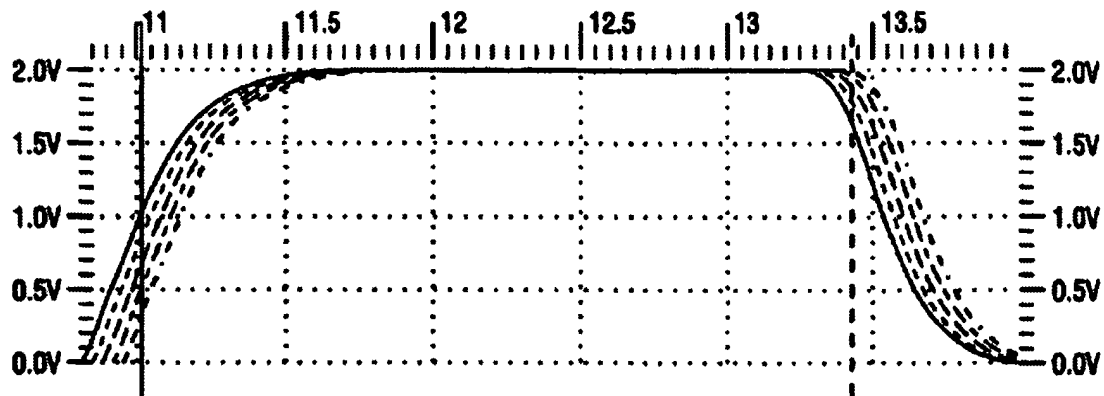
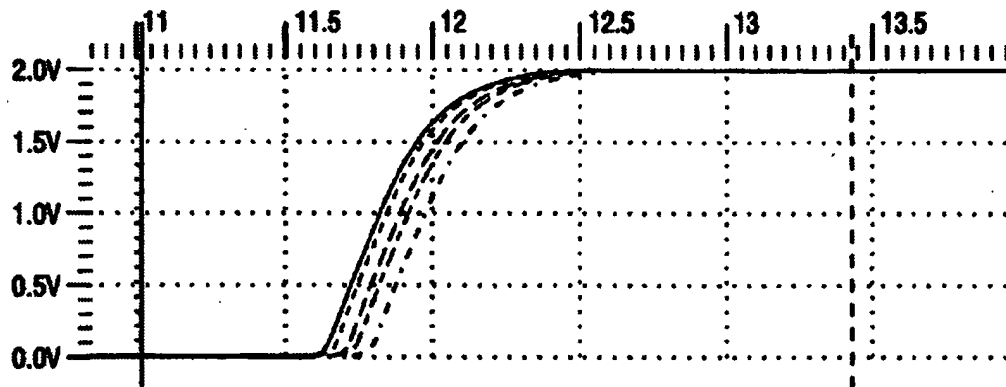
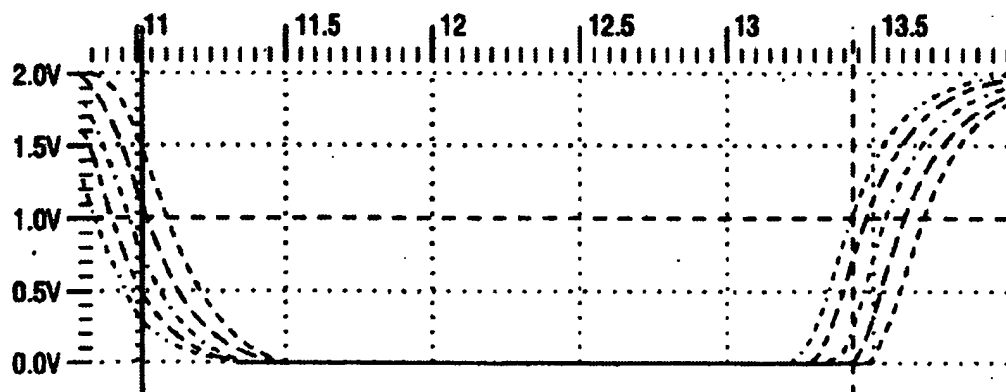
*Fig. 6**Fig. 7*

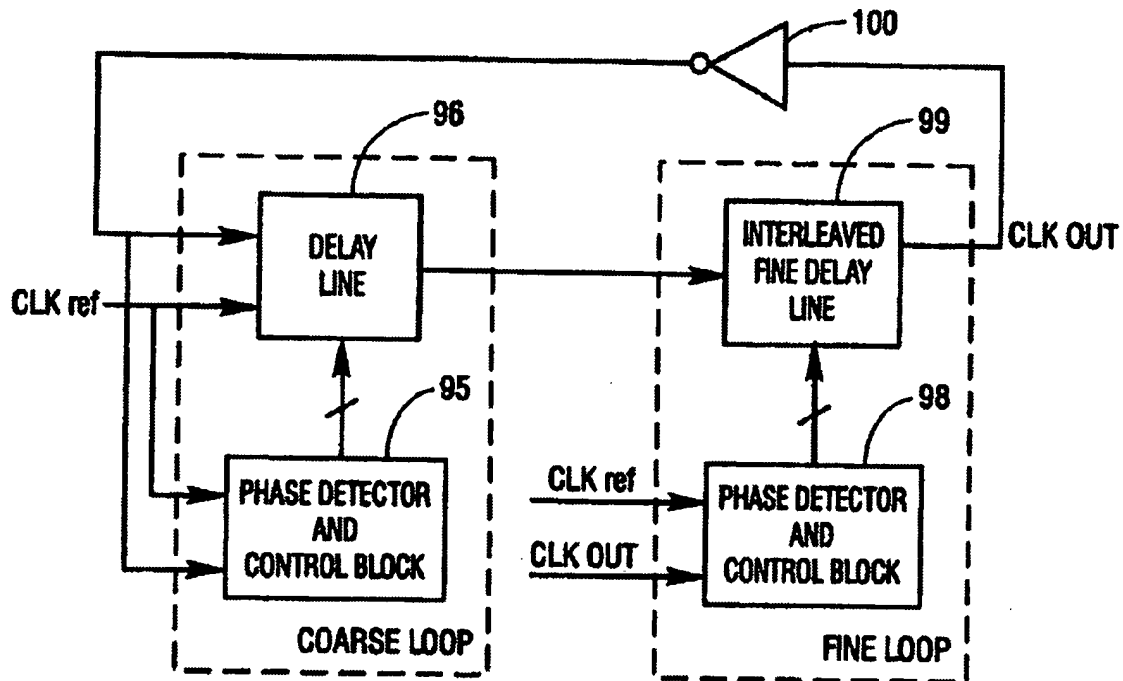
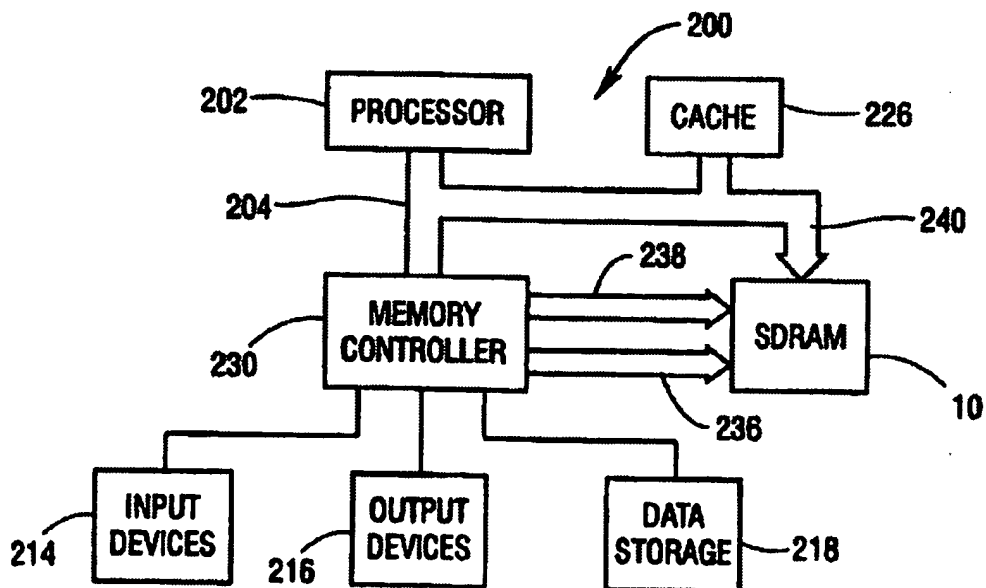
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**Fig. 8A****Fig. 8B****Fig. 8C**

*Fig. 9**Fig. 10*